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Temperature dependent negative capacitance behavior of Al/rhodamine-101/*n*-GaAs Schottky barrier diodes and R_s effects on the *C*–*V* and *G*/*ω*–*V* characteristics

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ABSTRACT

In order to explain the origin of negative capacitance, we have investigated the capacitance–voltage (*C*–*V*) and conductance–voltage (*G*/*ω*–*V*) measurements of the Al/rhodamine-101/*n*-GaAs Schottky barrier diodes (SBDs) in the temperature range of 110–290 K at 1 MHz by considering the series resistance (R_s) effect. Experimental results show that the values of *C* and *G*/*ω* were found to be strong functions of temperature and bias voltage. A strong negative capacitance (NC) phenomenon has been observed in the *C*–*V* plot for each temperature. It is clear that, the value of NC decreases with the increasing temperature at forward bias voltage and this decrease of the NC corresponds to an increase in the conductance. Such behavior of *C* in the forward bias region can be explained by the loss of interface charges localized at metal/semiconductor interface because of impact ionization process. Also, the magnitude of R_s makes a negative contribution to the low temperature capacitance. In addition, the high frequency *C* and *G*/*ω* values measured under reverse and forward bias were corrected by eliminating the effect of R_s to obtain the real diode capacitance.

1. Introduction

Metal-semiconductor (MS) and metal-insulator/polymer-semiconductor (MIS) types SBDs are the most widely used rectifying contacts in the electronic industry [1–4]. Especially, gallium arsenide (GaAs)-based structures are used as a basic component for high speed electronic, optoelectronic and low power devices [2,4–6]. Because of their technical importance, these devices have been thoroughly investigated [1–9] for four decades. However, the whole description of the current-transport mechanism of these devices is still a challenging problem. The current conduction mechanisms in these devices depend on various parameters. Especially, the series resistance (R_s) of device and organic interfacial layer at *M*/*S* interface play an important role in the *C*–*V* and *G*/*ω*–*V* characteristics [10–21]. R_s is one of the important sources of small signal energy loss in MS and MIS structures [6,7,10] and it can stem from five different sources: (1) the contact made by the probe wire to the gate; (2) the back contact of semiconductor; (3) impurities in semiconductor; (4) the resistance of quasi-neutral bulk semiconductor; and (5) non-uniform doping distribution in the semiconductor.

In the idealized case, the *C* of the structures is usually frequency independent, at high frequencies ($f \geq 1$ MHz), but the situation is different at low frequencies. Also, the admittance measurements of structures only at room temperature cannot give detailed information about their conduction mechanisms. Therefore, the investigation of *C*–*V* and *G*/*ω*–*V* characteristics in the wide temperature range is very important to understand the conduction mechanisms. The remarkable interest in the electrical and optical properties of organic molecular semiconductors reflects their increasingly widespread use in organic and hybrid inorganic–organic devices [2,8,9,22,23]. The modified GaAs Schottky diodes by reducing the interaction between metals and GaAs by organic interfacial layers are of considerable interest in high frequency applications [2,22,23].

In recent years, some investigations have reported a NC phenomenon in the forward bias *C*–*V* characteristics of some devices. These devices include MS diodes [24,25], hetero-junctions [3,26], far-infrared detectors [27], laser diodes [28], light emitting diodes [29], photo-detector [30] and some organic semiconductor devices [31]. This physical mechanism of the NC in different devices is obviously different. The observation of NC is important because it implies that an increment of bias voltage produces a decrease in

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the charge on the electrodes [24]. The term of NC means that the material displays an inductive behavior. In practice, explanation of the NC can be based on the behavior of temperature and frequency dependent admittance spectroscopy (C–V and G/ω–V) data [3,25]. The theory is established on following arguments. Electrons that surmount the Schottky barrier (SB) under forward bias do fill up the empty states at the interface, but they possess excess energy, when colliding with the electrons trapped at the N_{ss} they could also knock electrons out of the traps, provided that the binding energy of these traps is smaller than the SB energy. It is well known many electronic devices consist of a semiconductor between rectifier and ohmic contacts with N_{ss} and bulk traps where charges can be stored and released when an appropriate forward applied bias and external a.c. oscillation voltage are applied and thus a large effect can be produced on devices [24,32]. Although it is believed that the injection of charge carriers involves a process of hopping to localized interface traps/states, detailed physical mechanisms of injection are not well understood yet. However, Zhu et al. [29] show that the junction capacitance C is a differential effect of charge Q with respect to junction voltage V_j, i.e. $C = dQ/dV_j$. When the forward bias voltage reaches a certain value, the effect of the radiative recombination exceeds that of diffusion. Thus, the junction capacitance will become negative because dV_j is always positive. At high forward bias, the junction voltages tend to saturate, which means the small value of dV_j and the large value of C. In a real diode, the minority carrier intensity increases exponentially with forward bias, moreover, as more carriers are injected, the recombination velocity gets stronger. Therefore, the value of capacitance reaches to a maximum and then decreases rapidly to negative.

In this study, the forward and reverse bias C–V and G/ω–V characteristics of Al/rhodamine-101/n-GaAs structures have been investigated in a wide range of temperature (110–290 K) and applied bias voltage (−4 V to +5 V) at 1 MHz. Experimental results show that the values of C and G/ω are strong functions of temperature especially at forward bias region and we observed the NC after about 1. 75 V. In addition, to obtain the real C and G/ω values, the measured under reverse and forward bias capacitance (C_m) and conductance (G_m/ω) values were corrected as C_c and G_c/ω by eliminating the effect of R_s.

2. Experimental details

N-type GaAs wafer used for the fabrication of the Al/Rh101/n-GaAs SBDs has (1 0 0) orientation and 7.3×10^{15} cm^{-3} carrier concentration. The wafer was dipped in $5H_2SO_4 + H_2O_2 + H_2O$ solution for 1.0 min and then in $H_2O + HCl$ solution and then followed by a rinsing step in de-ionized water of 18 MΩ. After etching process Au–Ge (88%, 12%) for ohmic contact was evaporated on the back of the wafer in a vacuum-coating unit of 10^{-5} Torr. To form low resistivity ohmic contact, wafer was formed by thermal annealing at 450 °C for 3 min in N_2 ambient. Then the substrates were inserted into the vacuum system, and the Rh101 was evaporated on the front surface of the substrates by using a resistance heater. The Schottky contacts have been formed by evaporating Al as dots with diameter of about 1.5 mm on the front surface of the n-GaAs. The C–V and G/ω–V measurements of the Al/Rh101/n-GaAs SBDs were performed using a computerized controlled an HP4192 A LF impedance analyzer (5 Hz to 13 MHz) at 1 MHz in the temperature range of 110–290 K. The measurements were carried out in the Janes vpf-475 cryostat and temperature was controlled by using a Lake Shore model 321 auto-tuning temperature controller with sensitivity better than ±0.1 K.

3. Results and discussion

The C–V and G/ω–V characteristics of Al/Rh101/n-GaAs SBDs have been investigated in the temperature range of 110–290 K and at 1 MHz. Because at sufficiently high frequencies ($f \geq 1$ MHz), interface states cannot follow the ac signal [33]. The C–V and G/ω–V plots of the Al/Rh101/n-GaAs SBD are given in Fig. 1(a) and (b), respectively. As shown in Fig. 1(a) and (b), both C–V and G/ω–V characteristics exhibit accumulation, depletion and inversion regions. Negative capacitance (NC) phenomenon has been observed in the

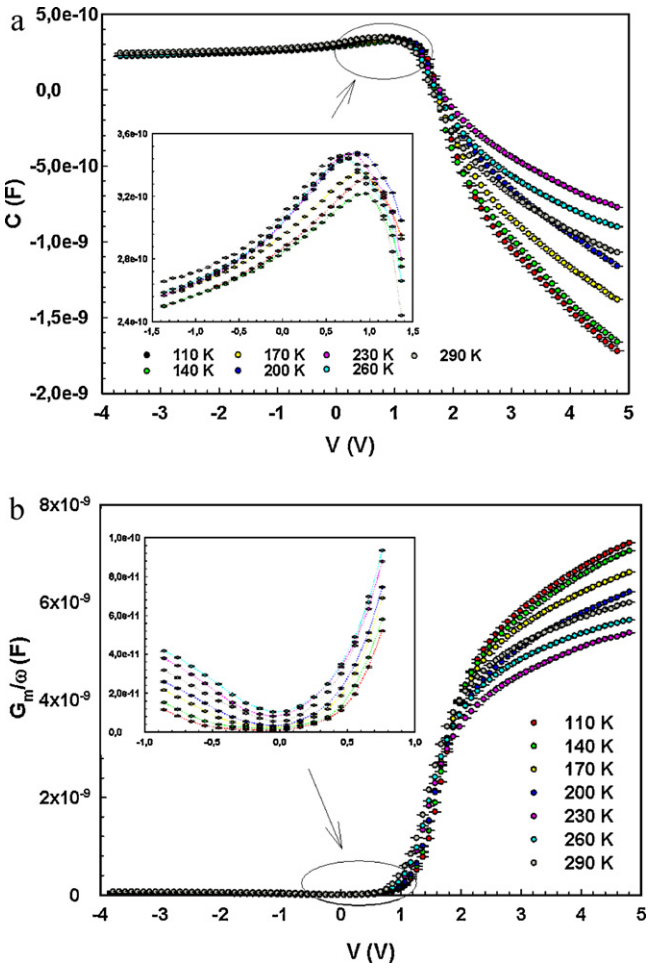

Fig. 1. The measured (a) capacitance $C_m(V,T)$ and (b) conductance $G_m(V,T)$ vs. applied bias voltage at various temperatures for Al/Rh101/n-GaAs SBD.

C–V plot for each temperature at higher bias voltage region due to the loss of interface charges localized at M/S interface. The values of the C increase with the increasing applied bias voltage and have a peak value in a certain bias region because of the existence of interface states and series resistance (R_s) [3,4,6,9,34]. On the other hand, the G/ω values decrease with the increasing temperature in the high forward bias voltages for the low temperatures ($T \leq 230$ K). When temperature is increased, the generation of thermal carriers (electrons or holes) in semiconductor is enhanced at both positive and negative biased conditions. Thus, the change in C values with the temperature especially at depletion and accumulation regions can be understood through charge storage ($C = Q/V$). The negative behavior of C is called "negative capacitance" (NC). Normally, such behavior of C with temperature cannot be explained by the ideal depletion and accumulation regions capacitance. Therefore, device's depletion region capacitance must not take negative capacitance values. Also, as can be seen from Fig. 1(a) and (b), the NC values appear at every temperature and correspond to the maximum of the SBD conductance. Such behavior of C–V–T and G/ω–V–T plots show that the material displays an inductive behavior [32,34]. According to Wu et al. [25] such behavior of C in the forward bias region can be explained by the loss of interface charges localized at metal/semiconductor interface due to impact ionization process. Similar results of the NC behavior have been reported in the literature [27–32]. Several suggestions have been proposed for the exact origin of NC [24–31,35]. Among them Jones et al. [24] stated that relaxation-like material is responsible for NC because of the

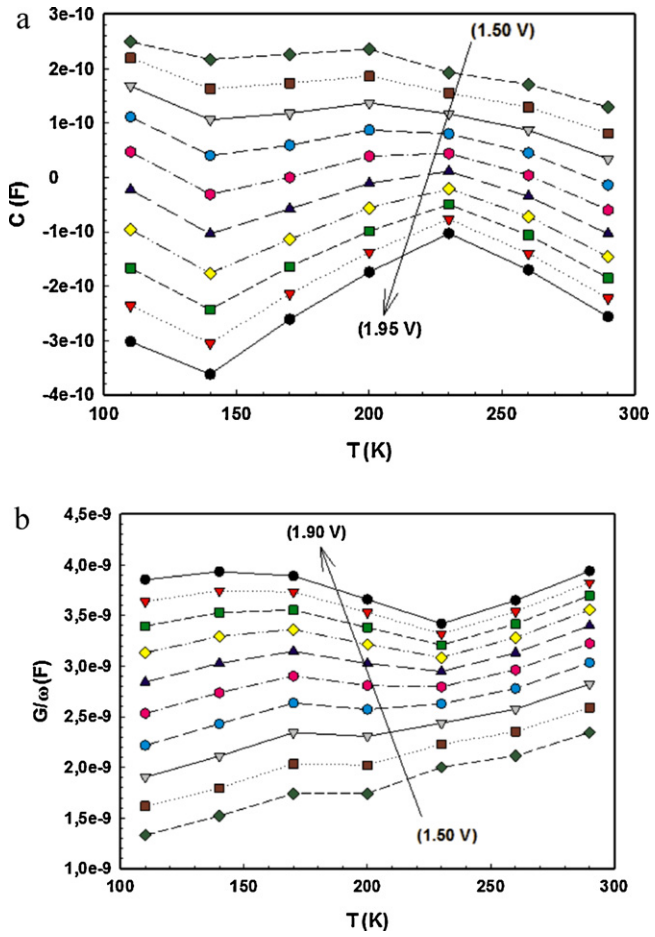

Fig. 2. The experimental (a) C and (b) G/ω characteristics of the Al/Rh101/n-GaAs SBD in the voltage range of 1.50–1.95 V with the step of 0.05 V.

injection of holes which recombine easily with the free electron charge of the dipole at M/S interface, also another origin of NC may be high resistivity materials, and it has been clearly shown by them [24]. In addition, it is believed that the NC caused by the injection of minority carriers can be observed only at forward applied bias voltage [3,36,37]. On other hand, it is believed that the injection of charge carriers involves a process of hopping to localized interface traps/states, but detailed physical mechanisms of injection are not understood fully until now.

In order to explain the effect of bias voltage, the capacitance and conductance values are given in Fig. 2(a) and (b) in the depletion region as a function of temperature with a bias voltage step of 0.05 V, respectively. We observed that the values of C decrease while those of G/ω increase with the increasing applied bias voltage. Such behavior of G/ω can be attributed to the increase in the number of charges under temperature effect depending on the relaxation time of the interface states. The changes in the values of C–T and G/ω–T plots become important especially at low temperatures and they increase with the increasing applied bias voltage. Another reason of such behavior of C–T and G/ω–T may be the re-structuring and re-ordering of charges at surface and interface traps. In other words, it is believed that the trap charges have enough energy to evacuate the traps located between metal and semiconductor interface in the Al/Rh101/n-GaAs bad gap at high temperatures.

According to the method presented by Nicollian and Brews [33], the real R_s of the SBDs can be determined from the measured capacitance (C_m) and conductance (G_m) in the strong accumulation region at high frequencies ($f \geq 1$ MHz). In addition, the voltage dependent value of R_s can be obtained from the measured C_m and

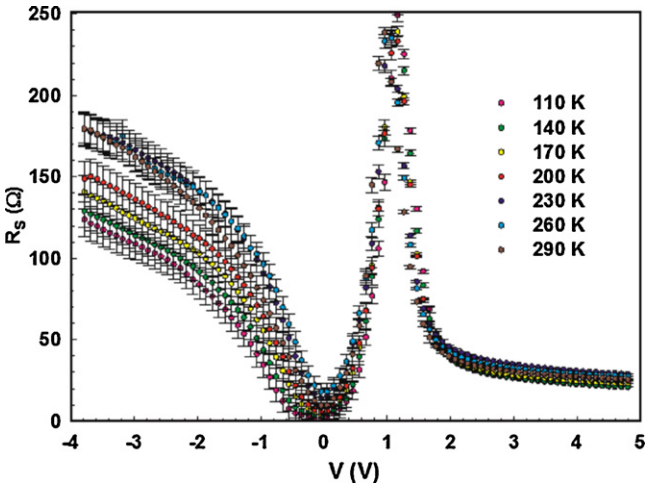

Fig. 3. R_s vs. V plots for Al/Rh101/n-GaAs SBD at various temperatures.

G_m values for given any bias voltage. The R_s correction of the capacitance (C_c) and conductance (G_c) is given by the following relations

$$C_c = \frac{[G_m^2 + (\omega C_m)^2]C_m}{a^2 + (\omega C_m)^2} \quad (1a)$$

and

$$G_c = \frac{[G_m^2 + (\omega C_m^2)]a}{a^2 + (\omega C_m)^2} \quad (1b)$$

where a and R_s are given in the following form.

$$a = C_m - [G_m^2 + (\omega C_m)^2]R_s \quad (2a)$$

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \quad (2b)$$

The R_s value of Al/Rh101/n-GaAs SBD was calculated according to Eq. (2b) and shown in Fig. 3 for various temperatures, and the temperature dependence of R_s for different forward biases at 1 MHz was also plotted in Fig. 4. These very significant values demanded that special attention should be given to the effects of the R_s in the C–V and G/ω–V characteristics, especially at high frequencies. As can be seen in Fig. 3, the R_s–V plots give a peak at about 1 V for each temperature and the peak position of R_s shifts towards to negative bias region. However, the peak magnitude is independent of temperature. Such behavior of the forward bias R_s–V peak

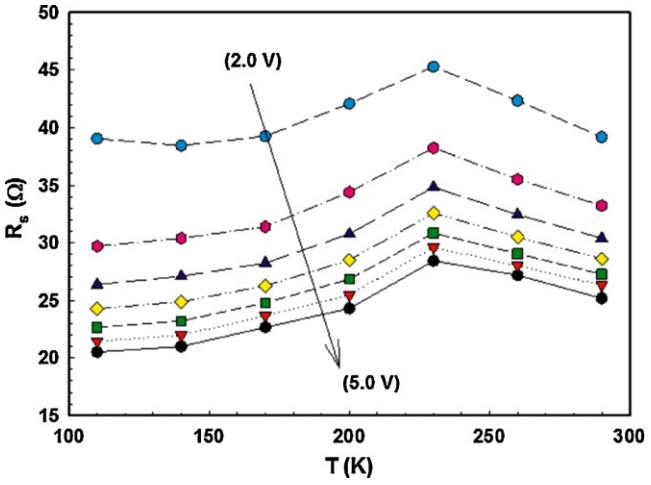

Fig. 4. The experimental temperature dependence of R_s for Al/Rh101/n-GaAs SBD at the voltage range 2–5 V with the step of 0.5 V.

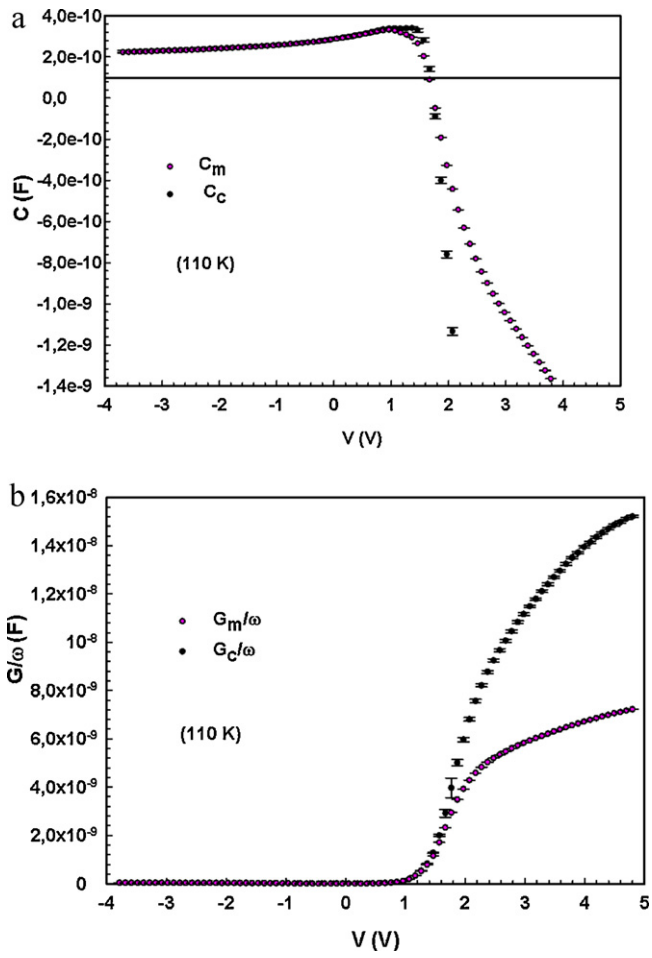

Fig. 5. The voltage dependent corrected (a) C_c–V and (b) G_c/ω–V plots of the Al/Rh101/n-GaAs SBD at 110 K.

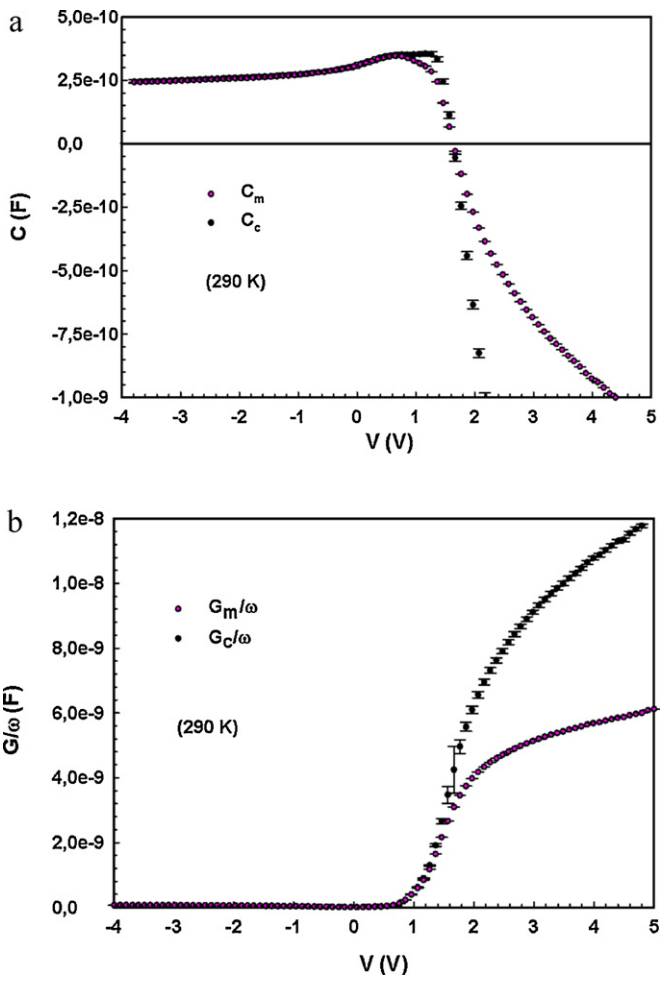

Fig. 6. The voltage dependent corrected (a) C_c–V and (b) G_c/ω–V plots of the Al/Rh101/n-GaAs SBD at 290 K.

can be attributed to the particular distribution of interface states at organic/semiconductor interface. Also, such behavior of R_s shows that the trap charges have enough energy to escape from the traps located between metal and semiconductor interface in the GaAs band gap. In this case, the R_s seems to be the most important parameter which causes the electrical characteristics of SBDs to be non-ideal.

In order to obtain the real diode C_c and G_c/ω values, the measured capacitance (C_m) and conductance (G_m/ω) values were corrected by eliminating the effect of R_s using Eqs. (1a) and (1b), and are given in Figs. 5 and 6 for 110 K and 290 K, respectively. After the correction step, the values of the C_c increase with the increasing voltage. It is clear that the values of C especially in the accumulation region almost get rid of negative value. This is a proof of the effect of R_s on the negative behavior of capacitance with voltage. Also, we believed that the magnitude of R_s leads to a negative contribution to the low temperature capacitance. On the other hand, in the accumulation region there is almost no change in the corrected values of G_c/ω–V.

In order to compare the variation of C and G/ω in the same bias voltage, the C–V and G/ω–V plots for the Al/Rh101/n-GaAs SBD are given in Figs. 7 and 8 for 110 K and 290 K, respectively. As can be seen in both figures, the values of C almost decrease with the increasing bias voltage for the given temperatures especially in the accumulation region. The decrease in C means that the dielectric constant of interfacial layer at M/S interfaces, whether native or deposited, decreases with measured temperature because of the polarization mechanism. Also, it can be attributed to the trap charges which have enough energy to escape from the traps localized at M/S interface. On the contrary, the values of conductance increase with the increasing bias voltage but decrease with the increasing temperature in the same regions. It can clearly be seen in Figs. 7 and 8 that the decrease in the capacitance corresponds to the increase in the conductance. On the other hand, the minimum of the C values coincides with the maximum of the conductance. It is well known, the existence of localized interface states between metal and semiconductor results in a charge dipole at interface.

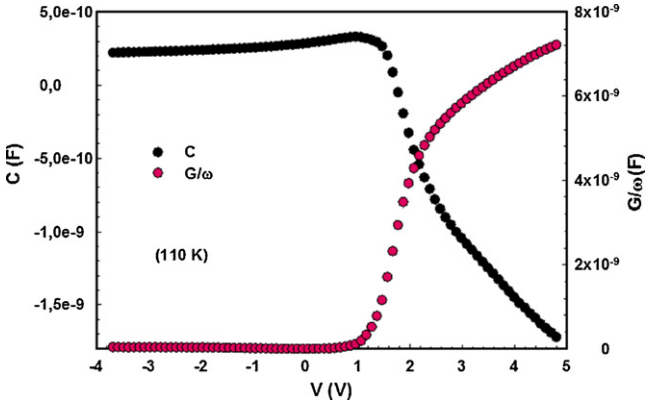

Fig. 7. The variation of the C–V and G/ω–V for the Al/Rh101/n-GaAs SBD as a function of bias voltage at 110 K.

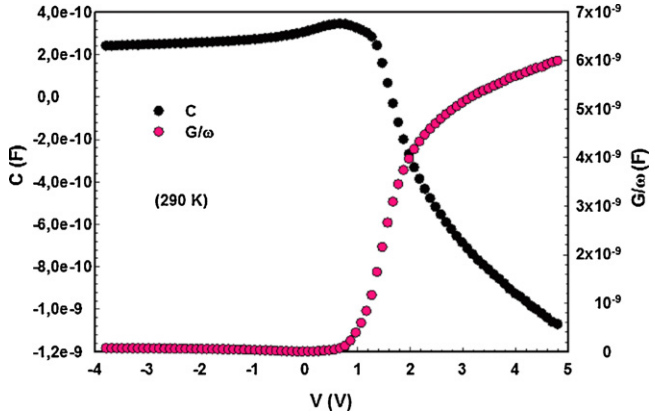

Fig. 8. The variation of the C–V and G/ω–V for the Al/Rh101/n-GaAs SBD as a function of bias voltage at 290 K.

Under forward bias, most of the applied bias voltage across the diode is shared by the semiconductor, series resistance of devices and interfacial dipole [23]. Therefore, it is thought that the capacitance values decrease with the increasing polarization and more carriers are introduced in the structure.

In conclusion, as far as we know, the studies on negative capacitance in GaAs SBDs are insufficient. Because, in the GaAs based structures, the C–V plot goes to negative at high forward bias region, especially, at low frequencies and temperatures. In addition, the negative capacitance was observed in the GaAs homojunction far-infrared detector Shen and Perera [27] and Perera et al. [36]. They showed that the magnitude of negative capacitance in the forward bias region decreases with the increasing temperature. They explained the origin of negative capacitance in terms of contact injection, interface states and minority carrier injection effects. On the other hand, according to Champness and Clark [37] the negative capacitance can be observed only at forward biases and low frequencies.

4. Conclusions

The negative capacitance in Al/rhodamine-101/n-GaAs SBDs has been investigated by using the C–V and G/ω–V measurements in the temperature range of 110–290 K at 1 MHz. Experimental results confirmed that both C and G/ω values are quite sensitive to the temperature. Negative capacitance (NC) phenomenon has been observed in the C–V plot for each temperature at higher bias voltage region due to the loss of interface charges localized at M/S interface. We observed that the value of NC decreases while G/ω increases with the increasing temperature. The R_s is also an important parameter which causes a change in the C and contributes to the negativity of low temperature capacitance. Therefore, the measured high frequency C and G/ω values should be corrected by eliminating the effect of R_s to obtain the real diode capacitance.

References

[1] H. Korkut, N. Yıldırım, A. Türüt, Physica B 404 (2009) 4039.
[2] Ö. Vural, Y. Şafak, Ş. Altındal, A. Türüt, Curr. Appl. Phys. 10 (2010) 761.
[3] E. Arslan, Y. Şafak, Ş. Altındal, Ö. Kelekçi, E. Özbay, J. Non-Cryst. Solids 356 (2010) 1006.
[4] P. Cattopadyay, Solid State Electron. 37 (1994) 1759.
[5] S.M. Sze, Physics of Semiconductor Devices, second ed., Wiley, New York, 1981.
[6] E.H. Rhoderick, R.H. Williams, Metal–Semiconductor Contacts, second ed., Clarendon, Oxford, 1978.
[7] Ş. Karataş, M. Çakar, Synth. Met. 159 (2009) 347.
[8] A.F. Özdemir, D.A. Aldemir, Ali Kökce, S. Altindal, Synth. Met. 159 (2009) 1427.
[9] İ. Dökme, Ş. Altındal, T. Tunç, İ. Uslu, Microelectron. Reliab. 50 (2009) 39.
[10] I. Nikitina1, K. Vassilevski, A. Horsfall, N. Wright, A.G. O'eill, S.K. Ray, K. Zekentes, C.M. Johnson, Semicond. Sci. Technol. 24 (2009) 055006.
[11] J.H. Werner, H.H. Güttler, J. Appl. Phys. 69 (1991) 1522.
[12] Y.P. Song, R.L. Van Meirhaeghe, W.H. Laflere, F. Cardon, Solid-State Electron. 29 (1986) 633.
[13] S. Chand, S. Bala, Appl. Surf. Sci. 252 (2005) 358.
[14] S.Y. Zhu, C. Detavernier, R.L. Van Meirhaeghe, G.P. Ru, X.P. Qu, B.Z. Li, F. Cardon, Solid-State Commun. 112 (1999) 611.
[15] Zs.J. Horvath, Solid State Electron. 39 (1996) 176.
[16] F.E. Jones, B.P. Wood, J.A. Myers, C.H. Daniels, M.C. Lonergan, J. Appl. Phys. 86 (1999) 6431.
[17] A. Bengi, H. Uslu, T. Asar, Ş. Altındal, S.Ş. Çetin, T.S. Mammadov, S. Özçelik, J. Alloys Compd. 509 (2011) 2897.
[18] H. Uslu, Ş. Altındal, U. Aydemir, İ. Dökme, İ.M. Afandiyeva, J. Alloys Compd. 503 (2010) 96.
[19] Ö. Demircioğlu, Ş. Karataş, N. Yıldırım, Ö.F. Bakkaloğlu, A. Türüt, J. Alloys Compd. 509 (2011) 6433.
[20] G.B. Sakr, I.S. Yahia, J. Alloys Compd. 503 (2010) 213.
[21] A. Bengi, U. Aydemir, Ş. Altındal, Y. Özen, S. Özçelik, J. Alloys Compd. 505 (2010) 628.
[22] M. Çakar, Y. Onganer, A. Türüt, Synth. Met. 126 (2002) 213.
[23] M. Çakar, C. Temirici, A. Türüt, Synth. Met. 142 (2004) 177.
[24] B.K. Jones, J. Santana, M. McPherson, Solid State Commun. 107 (1998) 47.
[25] X. Wu, E.S. Yang, H.L. Evans, J. Appl. Phys. 68 (1990) 2845.
[26] C.C. Wang, G.Z. Liu, M. He, H.B. Lu, Appl. Phys. Lett. 92 (2008) 052905.
[27] W.Z. Shen, A.G.U. Perera, Appl. Phys. A 72 (2001) 107.
[28] L.F. Feng, D. Li, C.Y. Zhu, C.D. Wang, H.X. Cong, X.S. Xie, C.Z. Lu, J. Appl. Phys. 102 (2007) 063102.
[29] C.Y. Zhu, L.F. Feng, C.D. Wang, H.X. Cong, G.Y. Zhang, Z.J. Yang, Z.Z. Chen, Solid State Electron. 53 (2009) 324.
[30] R. Gharbi, M. Abdelkrim, M. Fathllah, E. Tresso, S. Ferrero, C.F. Piri, T. Mohamed Brahim, Solid State Electron. 50 (2006) 367.
[31] E. Ehrenfreund, C. Lungenschmied, G. Dennler, H. Neugebauer, N.S. Sariciftci, Appl. Phys. Lett. 91 (2007) 012112.
[32] S. Noor Mohammad, Z.F. Fan, A.E. Botchkarev, W. Kim, O. Aktas, H. Markoç, F. Shiwei, K.A. Jones, M.A. Derenge, Philos. Mag. B 81 (2001) 453.
[33] E.H. Nicollian, J.R. Brews, Metal Oxide Semiconductor (MOS) Physics and Technology, John Willey & Sons, New York, 1982.
[34] P. Chattopadhyay, B. Raychaudhuri, Solid State Electron. 35 (1992) 1023.
[35] T. Noguchi, M. Kitagawa, I. Taniguchi, Jpn. J. Appl. Phys. 19 (1980) 1423.
[36] A.G.U. Perera, W.Z. Shen, M. Ershov, H.C. Liu, M. Buchanan, W.J. Schaff, Phys. Rev. Lett. 74 (1999) 3167.
[37] C.H. Champness, W.R. Clark, Appl. Phys. Rev. Lett. 56 (1990) 1104.